loop Project Status (06/27/2011 - 15:24:09)			
Project File:	eksblowfish_loop_2.xise	**Parser Errors:**	No Errors
Module Name:	eksblowfish_loop_2	**Implementation State:**	Placed and Routed
Target Device:	xc6slx45-3csg324	• **Errors:**	No Errors
Product Version:	ISE 13.1	• **Warnings:**	12 Warnings (12 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	X 1 Failing Constraint
Environment:	System Settings	• **Final Timing Score:**	656 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	1,145	54,576	2%	
Number used as Flip Flops	1,145			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	2,649	27,288	9%	
Number used as logic	2,644	27,288	9%	
Number using O6 output only	2,597			
Number using O5 output only	1			
Number using O5 and O6	46			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number used exclusively as route-thrus	5			
Number with same-slice register load	5			
Number with same-slice carry load	0			
Number with other load	0			
Number of occupied Slices	809	6,822	11%	
Number of LUT Flip Flop pairs used	2,675			
Number with an unused Flip Flop	1,544	2,675	57%	
Number with an unused LUT	26	2,675	1%	
Number of fully used LUT-FF pairs	1,105	2,675	41%	
Number of unique control sets	17			
Number of slice register sites lost to control set restrictions	71	54,576	1%	
Number of bonded IOBs	115	218	52%	
Number of RAMB16BWERs	2	116	1%	
Number of RAMB8BWERs	1	232	1%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	0	376	0%	
Number of BSCANs	0	4	0%	

Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	6.08			

Performance Summary			[-]
Final Timing Score:	656 (Setup: 656, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	X 1 Failing Constraint		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	seg 27. jun 15:20:47 2011	0	11 Warnings (11 new)	3 Infos (3 new)
Translation Report	Current	seg 27. jun 15:20:53 2011	0	0	0
Map Report	Current	seg 27. jun 15:23:00 2011	0	1 Warning (1 new)	6 Infos (6 new)
Place and Route Report	Current	seg 27. jun 15:23:58 2011	0	0	4 Infos (4 new)
Power Report					
Post-PAR Static Timing Report	Current	seg 27. jun 15:24:08 2011	0	0	3 Infos (3 new)
Bitgen Report					

Secondary Reports			[-]
Report Name	**Status**	**Generated**	

Date Generated: 06/27/2011 - 15:24:10