E101TopLevel Project Status (06/27/2011 - 19:30:49)			
Project File:	bflike1-interface.xise	**Parser Errors:**	No Errors
Module Name:	E101TopLevel	**Implementation State:**	Programming File Generated
Target Device:	xc6slx45-3csg324	• **Errors:**	No Errors
Product Version:	ISE 13.1	• **Warnings:**	85 Warnings (23 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	723	54,576	1%	
Number used as Flip Flops	723			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	1,573	27,288	5%	
Number used as logic	1,541	27,288	5%	
Number using O6 output only	1,343			
Number using O5 output only	29			
Number using O5 and O6	169			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number used exclusively as route-thrus	32			
Number with same-slice register load	31			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	565	6,822	8%	
Number of LUT Flip Flop pairs used	1,693			
Number with an unused Flip Flop	1,019	1,693	60%	
Number with an unused LUT	120	1,693	7%	
Number of fully used LUT-FF pairs	554	1,693	32%	
Number of unique control sets	31			
Number of slice register sites lost to control set restrictions	101	54,576	1%	
Number of bonded IOBs	42	218	19%	
Number of LOCed IOBs	41	42	97%	
Number of RAMB16BWERs	4	116	3%	
Number of RAMB8BWERs	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	0	376	0%	

Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	5.38			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	seg 27. jun 19:28:31 2011	0	74 Warnings (23 new)	37 Infos (0 new)
Translation Report	Current	seg 27. jun 19:28:37 2011	0	4 Warnings (0 new)	0
Map Report	Current	seg 27. jun 19:29:24 2011	0	3 Warnings (0 new)	9 Infos (0 new)
Place and Route Report	Current	seg 27. jun 19:29:54 2011	0	3 Warnings (0 new)	0
Power Report					
Post-PAR Static Timing Report	Current	seg 27. jun 19:30:06 2011	0	0	2 Infos (0 new)
Bitgen Report	Current	seg 27. jun 19:30:27 2011	0	1 Warning (0 new)	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	seg 27. jun 19:27:41 2011	
WebTalk Report	Current	seg 27. jun 19:30:27 2011	
WebTalk Log File	Current	seg 27. jun 19:30:48 2011	

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