

slow_key_setup1 Project Status (06/16/2011 - 16:11:18)			
<b>Project File:</b>	bflike1.xise	<b>Parser Errors:</b>	No Errors
<b>Module Name:</b>	slow_key_setup1	<b>Implementation State:</b>	Placed and Routed
<b>Target Device:</b>	xc6slx45-3fgg484	<b>• Errors:</b>	No Errors
<b>Product Version:</b>	ISE 13.1	<b>• Warnings:</b>	<a href="#">338 Warnings (37 new)</a>
<b>Design Goal:</b>	Balanced	<b>• Routing Results:</b>	<a href="#">All Signals Completely Routed</a>
<b>Design Strategy:</b>	<a href="#">Xilinx Default (unlocked)</a>	<b>• Timing Constraints:</b>	<a href="#">X 1 Failing Constraint</a>
<b>Environment:</b>	<a href="#">System Settings</a>	<b>• Final Timing Score:</b>	1241 ( <a href="#">Timing Report</a> )

Device Utilization Summary <span style="float: right;">[-]</span>				
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	290	54,576	1%	
Number used as Flip Flops	3			
Number used as Latches	287			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	1,423	27,288	5%	
Number used as logic	1,423	27,288	5%	
Number using O6 output only	1,272			
Number using O5 output only	0			
Number using O5 and O6	151			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number of occupied Slices	443	6,822	6%	
Number of LUT Flip Flop pairs used	1,423			
Number with an unused Flip Flop	1,134	1,423	79%	
Number with an unused LUT	0	1,423	0%	
Number of fully used LUT-FF pairs	289	1,423	20%	
Number of unique control sets	36			
Number of slice register sites lost to control set restrictions	14	54,576	1%	
Number of bonded <a href="#">IOBs</a>	24	316	7%	
IOB Latches	10			
Number of RAMB16BWERS	0	116	0%	
Number of RAMB8BWERS	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	10	376	2%	
Number used as OLOGIC2s	10			
Number used as OSERDES2s	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	

Number of BUFPLLs	0	8	0%
Number of BUFPLL_MCBs	0	4	0%
Number of DSP48A1s	0	58	0%
Number of ICAPs	0	1	0%
Number of MCBs	0	2	0%
Number of PCILOGICSEs	0	2	0%
Number of PLL_ADVs	0	4	0%
Number of PMVs	0	1	0%
Number of STARTUPS	0	1	0%
Number of SUSPEND_SYNCs	0	1	0%
Average Fanout of Non-Clock Nets	5.49		

Performance Summary <span style="float: right;">[-]</span>			
<b>Final Timing Score:</b>	1241 (Setup: 1241, Hold: 0)	<b>Pinout Data:</b>	<a href="#">Pinout Report</a>
<b>Routing Results:</b>	<a href="#">All Signals Completely Routed</a>	<b>Clock Data:</b>	<a href="#">Clock Report</a>
<b>Timing Constraints:</b>	<b>X 1 Failing Constraint</b>		

Detailed Reports <span style="float: right;">[-]</span>					
Report Name	Status	Generated	Errors	Warnings	Infos
<a href="#">Synthesis Report</a>	Current	qui 16. jun 16:09:15 2011	0	<a href="#">301 Warnings (0 new)</a>	<a href="#">1 Info (0 new)</a>
<a href="#">Translation Report</a>	Current	qui 16. jun 16:09:21 2011	0	0	0
<a href="#">Map Report</a>	Current	qui 16. jun 16:10:23 2011	0	<a href="#">37 Warnings (37 new)</a>	<a href="#">6 Infos (0 new)</a>
<a href="#">Place and Route Report</a>	Current	qui 16. jun 16:10:59 2011	0	0	<a href="#">4 Infos (0 new)</a>
Power Report					
<a href="#">Post-PAR Static Timing Report</a>	Current	qui 16. jun 16:11:16 2011	0	0	<a href="#">3 Infos (0 new)</a>
<a href="#">Bitgen Report</a>	Out of Date	seg 30. mai 16:27:58 2011	0	0	0

Secondary Reports <span style="float: right;">[-]</span>		
Report Name	Status	Generated
<a href="#">ISIM Simulator Log</a>	Out of Date	seg 13. jun 18:44:17 2011
<a href="#">WebTalk Report</a>	Out of Date	seg 30. mai 16:27:58 2011
<a href="#">WebTalk Log File</a>	Out of Date	seg 30. mai 16:28:20 2011

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