E101TopLevel Project Status			
Project File:	eksblowfish_loop_interface.xise	**Parser Errors:**	No Errors
Module Name:	E101TopLevel	**Implementation State:**	Programming File Generated
Target Device:	xc6slx45-3csg324	**• Errors:**	No Errors
Product Version:	ISE 13.1	**• Warnings:**	70 Warnings (70 new)
Design Goal:	Balanced	**• Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	All Constraints Met
Environment:	System Settings	**• Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	1,572	54,576	2%	
Number used as Flip Flops	1,572			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	3,391	27,288	12%	
Number used as logic	3,349	27,288	12%	
Number using O6 output only	3,183			
Number using O5 output only	30			
Number using O5 and O6	136			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number used exclusively as route-thrus	42			
Number with same-slice register load	41			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	1,076	6,822	15%	
Number of LUT Flip Flop pairs used	3,508			
Number with an unused Flip Flop	2,003	3,508	57%	
Number with an unused LUT	117	3,508	3%	
Number of fully used LUT-FF pairs	1,388	3,508	39%	
Number of unique control sets	43			
Number of slice register sites lost to control set restrictions	148	54,576	1%	
Number of bonded IOBs	42	218	19%	
Number of LOCed IOBs	41	42	97%	
Number of RAMB16BWERs	6	116	5%	
Number of RAMB8BWERs	1	232	1%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	0	376	0%	

Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	5.48			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	seg 4. jul 18:42:15 2011	0	57 Warnings (57 new)	39 Infos (39 new)
Translation Report	Current	seg 4. jul 18:42:51 2011	0	4 Warnings (4 new)	0
Map Report	Current	seg 4. jul 18:46:04 2011	0	4 Warnings (4 new)	9 Infos (9 new)
Place and Route Report	Current	seg 4. jul 18:46:58 2011	0	3 Warnings (3 new)	0
Power Report					
Post-PAR Static Timing Report	Current	seg 4. jul 18:47:11 2011	0	0	2 Infos (2 new)
Bitgen Report	Current	seg 4. jul 18:47:37 2011	0	2 Warnings (2 new)	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	seg 4. jul 18:47:37 2011	
WebTalk Log File	Current	seg 4. jul 18:47:46 2011	

Date Generated: 07/04/2011 - 21:09:33