slow_key_setup1 Project Status (06/16/2011 - 15:57:29)			
Project File:	bflike1.xise	**Parser Errors:**	No Errors
Module Name:	slow_key_setup1	**Implementation State:**	Placed and Routed
Target Device:	xc6slx45-3fgg484	• **Errors:**	No Errors
Product Version:	ISE 13.1	• **Warnings:**	338 Warnings (37 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	290	54,576	1%	
Number used as Flip Flops	3			
Number used as Latches	287			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	938	27,288	3%	
Number used as logic	938	27,288	3%	
Number using O6 output only	763			
Number using O5 output only	0			
Number using O5 and O6	175			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number of occupied Slices	294	6,822	4%	
Number of LUT Flip Flop pairs used	943			
Number with an unused Flip Flop	654	943	69%	
Number with an unused LUT	5	943	1%	
Number of fully used LUT-FF pairs	284	943	30%	
Number of unique control sets	36			
Number of slice register sites lost to control set restrictions	14	54,576	1%	
Number of bonded IOBs	24	316	7%	
IOB Latches	10			
Number of RAMB16BWERs	0	116	0%	
Number of RAMB8BWERs	0	232	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	10	376	2%	
Number used as OLOGIC2s	10			
Number used as OSERDES2s	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	

Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	5.13			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	qui 16. jun 15:55:33 2011	0	301 Warnings (0 new)	1 Info (0 new)
Translation Report	Current	qui 16. jun 15:55:39 2011	0	0	0
Map Report	Current	qui 16. jun 15:56:48 2011	0	37 Warnings (37 new)	6 Infos (0 new)
Place and Route Report	Current	qui 16. jun 15:57:11 2011	0	0	4 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	qui 16. jun 15:57:27 2011	0	0	3 Infos (0 new)
Bitgen Report	Out of Date	seg 30. mai 16:27:58 2011	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
ISIM Simulator Log	Out of Date	seg 13. jun 18:44:17 2011	
WebTalk Report	Out of Date	seg 30. mai 16:27:58 2011	
WebTalk Log File	Out of Date	seg 30. mai 16:28:20 2011	

Date Generated: 06/16/2011 - 15:57:29