E101TopLevel Project Status			
Project File:	eksblowfish-loop-many.xise	**Parser Errors:**	No Errors
Module Name:	E101TopLevel	**Implementation State:**	Programming File Generated
Target Device:	xc6slx45-3csg324	• **Errors:**	No Errors
Product Version:	ISE 13.1	• **Warnings:**	76 Warnings (3 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	5,027	54,576	9%	
Number used as Flip Flops	5,027			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	14,043	27,288	51%	
Number used as logic	13,991	27,288	51%	
Number using O6 output only	13,329			
Number using O5 output only	29			
Number using O5 and O6	633			
Number used as ROM	0			
Number used as Memory	0	6,408	0%	
Number used exclusively as route-thrus	52			
Number with same-slice register load	51			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	4,490	6,822	65%	
Number of LUT Flip Flop pairs used	14,180			
Number with an unused Flip Flop	9,324	14,180	65%	
Number with an unused LUT	137	14,180	1%	
Number of fully used LUT-FF pairs	4,719	14,180	33%	
Number of unique control sets	112			
Number of slice register sites lost to control set restrictions	461	54,576	1%	
Number of bonded IOBs	42	218	19%	
Number of LOCed IOBs	41	42	97%	
Number of RAMB16BWERs	12	116	10%	
Number of RAMB8BWERs	4	232	1%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	8	0%	
Number of ILOGIC2/ISERDES2s	0	376	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	376	0%	
Number of OLOGIC2/OSERDES2s	0	376	0%	

Number of BSCANs	0	4	0%	
Number of BUFHs	0	256	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	58	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	4	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	6.44			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0, Component Switching Limit: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	seg 15. ago 21:25:44 2011	0	63 Warnings (1 new)	39 Infos (0 new)
Translation Report	Current	seg 15. ago 21:25:57 2011	0	4 Warnings (0 new)	0
Map Report	Current	seg 15. ago 21:31:49 2011	0	4 Warnings (2 new)	9 Infos (1 new)
Place and Route Report	Current	seg 15. ago 21:37:01 2011	0	3 Warnings (0 new)	0
Power Report					
Post-PAR Static Timing Report	Current	seg 15. ago 21:37:33 2011	0	0	2 Infos (0 new)
Bitgen Report	Current	seg 15. ago 21:38:34 2011	0	2 Warnings (0 new)	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	seg 15. ago 21:38:36 2011	
WebTalk Log File	Current	seg 15. ago 21:38:59 2011	

Date Generated: 08/16/2011 - 00:31:01